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Patent

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Application No	85115733	**Filing Date**	1996/12/20
Title	Multiple pocket implant for improved performance and channel length control of MOSFET properties		
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Priority Data

Country	**Application No**	**Priority Date**
US	19950006083P	1995/10/24

Patent Abstract

A method of forming a transistor, which comprises the following steps: forming a gate on a substrate; forming a first pocket region on at least one side of the gate, the concentration of a first species on the near surface of the first pocket region being higher than the concentration on the sub surface; forming a second pocket region on at least one side of the gate, the concentration of a second species on the near sub surface of the second pocket region being higher than the concentration on the near surface; and forming a source region and a drain region in the substrate on the opposite side of the gate.

BACK

85115733

TI-20055

TW 349248

PATENT APPLICATION

MULTIPLE POCKET IMPLANT FOR IMPROVED PERFORMANCE AND CHANNEL LENGTH CONTROL OF MOSFET PROPERTIES

CROSS-REFERENCE TO RELATED APPLICATION

The following co-pending application is hereby incorporated by reference:

Serial No.	Filed	Inventors
(TI-20072)		Chatterjee et al.

FIELD OF THE INVENTION

This invention generally relates to semiconductor processing and more specifically to short channel transistors.

BACKGROUND OF THE INVENTION

Today's smaller transistors (i.e., those having a channel length less than 0.5 microns) tend to suffer from problems with channel length control of MOSFET (metal-oxide-semiconductor field effect transistor) properties such as drain-induced barrier lowering (DIBL) and correspondingly, threshold voltage roll-off. DIBL can occur at the surface or below the surface (sub-surface: typically to a depth $\leq$ 1500Å). Both surface and sub-surface DIBL can lead to undesirably high MOSFET leakage current between the source and drain. It is noted that sub-surface DIBL is associated with (a) low net sub-surface dopant concentration between source and drain, and/or (b) low effective sub-surface separation between source and drain regions. Similarly, surface DIBL is associated with (a) low net dopant concentration at or near the surface between source and drain, and/or (b) low effective separation between source and drain regions at or near the surface. As an example of surface DIBL, it has been found that in p-type MOSFETS having

a channel 2 threshold adjust implant of arsenic to form a low surface concentration dopant and high sub-surface concentration (i.e., a retrograde profile), a significant source/drain dopant tail profile 4 exists at the surface of the device as shown in Figure 1. The diffusion tail profile can be detrimental to MOSFET performance by increasing the threshold voltage roll-off beyond that expected with no tail profile due to reasons (a) and (b) discussed above.

Pocket implants have been used to improve channel length control of MOSFET properties, but without significantly increasing dopant concentration in the entire channel region between the source and drain. The pocket implant is an additional dopant step that increases the dopant concentration adjacent to one or both of the source and drain regions at/near the ends of a MOSFET channel region. If a pocket implant is formed with, for example, an arsenic dopant, to form a retrograde pocket doping profile (as shown in Fig. 2a), then the high dopant concentration in the sub-surface region can prevent sub-surface DIBL. However, the low resultant dopant concentration in the surface or near-surface region may not sufficiently prevent surface DIBL. Conversely, if another dopant species such as phosphorous (and/or a low energy arsenic implant) is utilized to form a non-retrograde doping profile (i.e., high surface concentration and low sub-surface concentration as shown in Fig. 2b), then the high dopant concentration in the surface region can prevent surface DIBL. However, the low resultant dopant concentration in the sub-surface region may not sufficiently prevent sub-surface DIBL. Accordingly, a transistor and method are desired that optimally improve both (near) surface leakage and sub-surface leakage.

SUMMARY OF THE INVENTION

A transistor and method of forming a transistor is disclosed herein. The transistor comprises at least a two step pocket implant on either of or both of the source side and the drain side of the channel region. One step of the pocket implant ensures sufficient concentration near the surface of the transistor. The other step of the pocket implant ensures sufficient concentration in the sub-surface region of the transistor. Thus, both surface and sub-surface DIBL and threshold voltage roll-off are improved.

An advantage of the invention is providing a transistor having improved channel length control of MOSFET properties.

A further advantage of the invention is providing a transistor wherein both DIBL and threshold voltage roll-off are optimally improved.

These and other advantages will be apparent to those of ordinary skill in the art having reference to the specification in conjunction with the claims.

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PATENT APPLICATION

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a cross-sectional diagram of a prior art transistor having a source and drain dopant profile tail;

FIGs. 2a-b are graphs of dopant concentration versus depth in a substrate for prior art pocket implants;

FIG. 3 is a cross-sectional diagram of a PMOSFET having a multiple pocket implant according to the invention;

FIG. 4 is a graph of dopant concentration versus depth in a substrate according to the invention;

FIGs. 5-8 are cross-sectional diagrams of the multiple pocket implant MOSFET of FIG. 3 at various stages of fabrication.

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The invention will now be described in conjunction with a p-type MOSFET (PMOSFET). It will be apparent to those of ordinary skill in the art that the benefits of the invention may also be utilized with other types of transistors such as NMOSFET, and with either type of transistor having raised source/drains. Although the invention will be described as having the pocket implant adjacent the source side, the pocket implant may alternatively or additionally be formed on the drain side.

A PMOSFET 10 according to the invention is shown in Figure 3. PMOSFET 10 is formed in a n-type well (or substrate) 12. Gate electrode 14 is separated from well region 12 by a gate oxide layer 16. Source region 20 and drain region 22 are formed in well region 12 and, for a PMOSFET, comprise a p-type dopant. Channel region 24 is located below gate electrode 14.

On one side of channel region 24 is pocket implant region 26. Pocket region 26 may be located on the source side, the drain side, or one pocket region 26 may be located on the source side and another on the drain side. Pocket implant region 26 comprises two portions, upper portion 28 and lower portion 30. Upper portion 28 provides a higher dopant concentration at the surface to desirably reduce surface DIBL, similar to Fig. 1b. Lower portion 30 provides a higher dopant concentration in the sub-surface area to improve sub-surface DIBL, similar to Fig. 1a. Upper and lower portions 28 and 30 may comprises different species, the same species at different implant doses, same or different species implanted at different energies, same or different species implanted at different angles, or a combination of the above. The result is a pocket implant region 26 that has a sufficient dopant concentration both near the surface and in the sub-surface region. An exemplary dopant profile for the invention is shown in Fig. 4. Although Fig. 4 illustrates a flat dopant profile in the near surface and subsurface regions, a flat

dopant profile may not be neccessary as long as sufficient dopant exists in both the near-surface and sub-surface regions. The species concentration desired varies depending on many factors including the nominal gate length and power supply associated with the MOSFET technology being designed. Examples will be discussed below.

A method for forming the PMOSFET 10 according to an embodiment of the invention will now be described. First, the device is fabricated through the formation of gate electrode 14, as shown in Figure 5. A masking layer 32 is formed that exposes the area of substrate 12 where either the drain region or the source region is to be formed. If pocket region are desired on both sides, both the source and drain sides are exposed. A symetrical device having a pocket implant area 26 on both sides may be cheaper to fabricate. However, better performance may result by having a pocket implant area on only one side. In the preferred embodiment, the drain region is exposed, as shown in Figure 6. Advantages of placing the pocket implant area on the drain side are discussed in U.S. Patent Applicant No. (TI-20072), filed _____, and assigned to Texas Instruments, Inc. A first process is then used to form portion 28 of pocket implant area 26. A second process is used to form portion 30 of pocket implant area 26. Both portions 28 and 30 are shown in Fig. 7. Although shown as forming upper portion 28 first, the order may be reversed if desired and the second process to form lower portion 30 may be performed first. The first process is designed to place a higher concentration of species near the surface and the second process is designed to place a higher concentration of species in the bulk area. Concentrations in the range of 5E16 - 4E17 are desired near the surface and concentrations in the range of 2E17-1E18 are desired in the sub-surface region. The first and second processes may use different species, for example, phosphorous and arsenic respectively. Arsenic may be replaced with antimony. For a NMOSFET, phosphorous may be replaced with boron and arsenic may be replaced with indium. It is important to note that the species need not be a dopant, as long as the functions of cutting off a dopant tail and improving threshold voltage roll-off and DIBL are achieved. For example, a germanium or silicon species may be used.

Alternatively, the first process may be performed at a lower energy than the second process either with the same or different species. For example, upper portion 28 may be formed by implanting arsenic at a first energy level (e.g., 5-30 KeV) and the lower portion 30 may be formed by implanting arsenic at a second energy level greater than the first energy level (e.g., 80-180 KeV). Alternatively, phosphorous may be implanted at two different energy levels. If two species are desired, upper portion 28 may be formed by implanting phosphorous at one energy level (e.g., 5-50 KeV) and the lower portion may be formed by implanting arsenic at a second energy level higher than the first (e.g., 80-180 KeV). Of course, the energy level desired depends on many factors such as species type and implant dose. The key is that the implant rang associated with the second implant process is greater than the first.

Other methods for forming the upper and lower portions 28, 30 include using different implant dose levels and/or different implant angles for the first and second processes. Using implant dose levels, a higher dose level is used for the lower portion relative to the upper portion. If different implant angles are desired, the first process for forming the upper portion uses a higher angle than the second process.

It should be noted that any of the above suggestions may be combined to form the upper and lower portions 28,30. In the preferred embodiment, different species and energy levels are used. For example, phosphorous and arsenic are implanted with arsenic being implanted at a higher energy than the phosphorous. The arsenic implant may be a conventional pocket implant known as super-steep retrograde (SSR) implant. Then an additional implant of phosphorous is performed. Thus, the arsenic implant provides a high concentration at the desired depth in the substrate and the phosphorous implant provides a higher concentration near the surface.

At this point, sidewall spacers 36 may be formed if desired on the sidewalls of gate electrode 14, as shown in Figure 8. Sidewall spacers 36 typically comprise a dielectric material

such as silicon-oxide or silicon-nitride. Other suitable materials will be apparent to those skilled in the art. Then, source region 20 and drain region 22 are formed, for example, by ion implantation. Source region 20 and drain region 22 comprise p-type dopants. The dopant concentration will vary by design and may, for example, be in the range of 1E18 to 1E20/cm^3. It should be noted that source region 20 and drain region 22 and/or sidewall spacers 36 may be formed prior to pocket implant region 26. Furthermore, drain extension regions may be formed as is known in the art. The depth of pocket implant 26 is determined by that neccesary to prevent sub-surface leakage. Accordingly, the depth may be on the order of the depth of source and drain regions 20, 22.

It will be apparent to those skilled in the art that if a NMOSFET is desired, the conductivity types discussed above would be reversed. While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. For example, more than two implant processes may be utilized. It is therefore intended that the appended claims encompass any such modifications or embodiments.

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PATENT APPLICATION

WHAT IS CLAIMED IS:

1. A method of forming a transistor comprising the steps of:

forming a gate electrode on a substrate;

forming a first pocket region on at least one side of said gate electrode, said first pocket region having a higher concentration of a first species near a surface than in a sub-surface region:

forming a second pocket region on said at least one side of said gate electrode, said second pocket region having a higher concentration of a second species near said sub-surface region than near said surface; and

forming a source region and a drain region in said substrate on opposite sides of said gate electrode.

2. The method of claim 1, wherein said first species and said second species comprise the same species.

3. The method of claim 1, wherein said first species and said second species each comprise a dopant material.

4. The method of claim 1, wherein said first species comprises phosphorous and said second species comprises arsenic.

5. The method of claim 1, wherein said first species comprises boron and said second species comprises indium.

6. The method of claim 1, wherein said step of forming said first pocket region comprises the step of implanting said first species at a first energy level and said step of forming said second

pocket region comprises the step of implanting said second species at a second energy level, said second energy level being greater than said first energy level.

7. The method of claim 6, wherein said first species and said second species comprise the same species.

8. The method of claim 1, wherein said step of forming said first pocket region comprises the step of implanting said first species at a first angle and said step of forming said second pocket region comprises the step of implanting said second species at a second angle, said second angle being less than said first angle.

9. The method of claim 1, wherein said step of forming said first pocket region comprises the step of implanting said first species at a first implant dose and said step of forming said second pocket region comprises the step of implanting said second species at a second implant dose, said second implant dose being greater than said first implant dose.

10. The method of claim 1, wherein said step of forming said first pocket region comprises the step of implanting said first species at a first implant dose and said step of forming said second pocket region comprises the step of implanting said second species at a second implant dose, said second implant dose being less than said first implant dose.

11. The method of claim 1, wherein said first and second pocket regions are formed adjacent said source region.

12. The method of claim 1, wherein said pocket implant region is formed adjacent said drain region.

13. The method of claim 1, wherein said at least one side comprises both a source side and a drain side.

14. The method of claim 1, wherein said step of forming said second pocket region occurs prior to said step of forming said first pocket region.

15. The method of claim 1, wherein said step of forming said source and drain region occurs prior to said step of forming said first pocket region.

16. The method of claim 1, wherein said step of forming said source and drain regions occur after said step of forming said first pocket region and prior to said step of forming said second pocket region.

17. A method for forming a transistor, comprising the steps of:

forming a gate electrode over a substrate;

implanting a first species at a first energy level and first implant dose into at least one pocket area in said substrate adjacent at least one side of said gate electrode;

implanting a second species at a second energy level and a second implant dose into said at least one pocket area in said substrate on said at least one side of said gate electrode; and

forming a source region and a drain region on opposite sides of said gate electrode.

18. The method of claim 17, wherein said at least one pocket area comprises a first and a second pocket area, said first pocket area located on a source side of said gate and said second pocket area located on a drain side of said gate.

19. The method of claim 17, wherein said first energy level is less than said second energy level.

20. The method of claim 17, wherein said first implant dose is less than said second implant dose.

21. The method of claim 17, wherein said first species is implanted at a first angle and said second species is implanted at a second angle, said first angle being greater than said second angle.

22. A transistor comprising:

a gate electrode over a substrate;

two source/drain regions located on opposite sides of said gate electrode within said substrate; and

a first pocket implant region adjacent one of said source/drain regions within said substrate, said pocket implant region having a species profile that is less than an order of magnitude different between a sub-surface region and a near surface region.

23. The transistor of claim 22, wherein said pocket implant region comprises a first species having a greater concentration in said near surface region and a second species having a greater concentration in said bulk region.

24. The transistor of claim 22, wherein said first species comprises phosphorous and said second species comprises arsenic.

25. The transistor of claim 22, wherein said first species comprises boron and said second species comprises indium.

26. The transistor of claim 22, further comprising a second pocket implant region adjacent an opposite one of said source/drain regions from said first pocket implant region.

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PATENT APPLICATION

ABSTRACT

A transistor and method of forming a transistor. The transistor (10) comprises a source region (20) and a drain region (22) located in a substrate (12). The transistor (10) also comprises a pocket implant region (26) having an upper portion (28) and a lower portion (30). The upper portion (28) provides a higher species concentration near the surface. The lower portion (30) provides a higher species concentration near the bulk region. Thus, DIBL and threshold voltage roll-off are both improved.

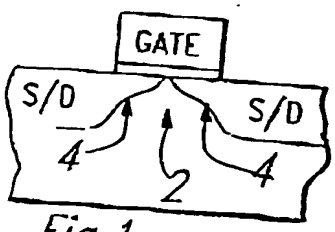

Fig.1

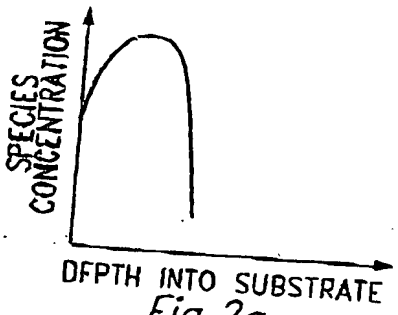

Fig.2a

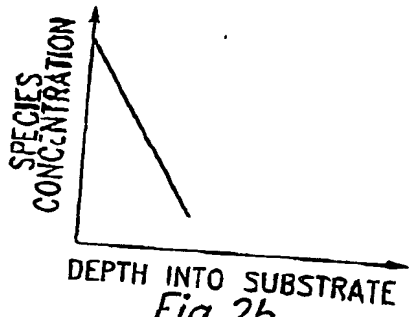

Fig.2b

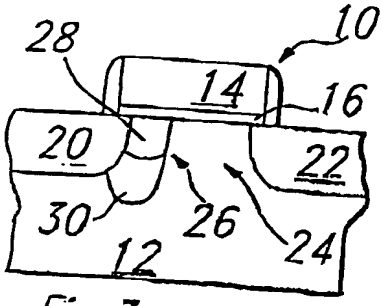

Fig.3

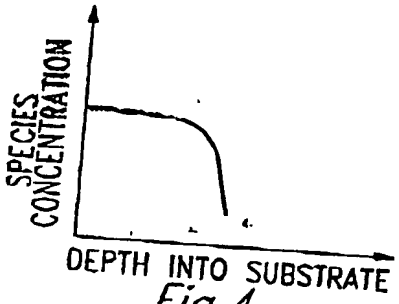

Fig.4

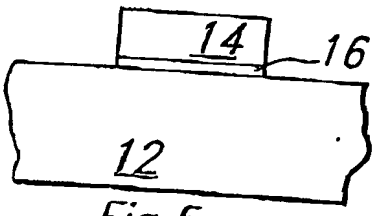

Fig.5

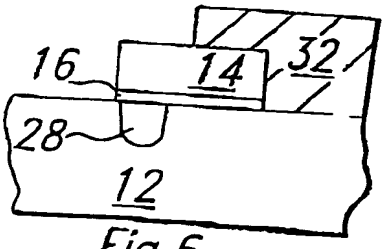

Fig.6

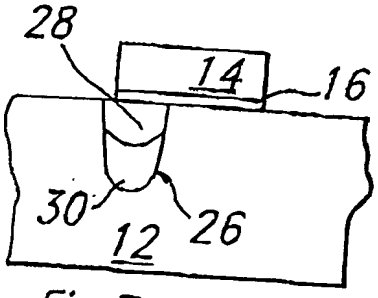

Fig.7

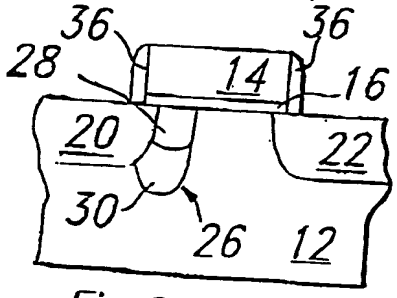

Fig.8